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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,191	08/02/2006	Masayoshi Kinoshita	071971-0690	6782

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EXAMINER	
COLE, BRANDON S	

ART UNIT	PAPER NUMBER
4125	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,191	KINOSHITA ET AL.	
	Examiner	Art Unit	
	BRANDON S. COLE	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/02/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1–3, 5 , and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as in view of Chou (US 6,201,435)

As to claim 1 AAPA figure 7 shows a reference voltage generation circuit for generating a constant reference voltage at a reference voltage output terminal (0), comprising: a first diode element (D1) having a cathode connected to a ground potential; a second diode element (D2) which has a current density different from that of

the first diode element and whose cathode is connected to the ground potential; a first resistive element (R1) having an end connected to an anode of the second diode element; a second resistive element (R2) having an end connected to the other end of the first resistive element, the other end of the second resistive element being connected to the reference voltage output terminal; a third resistive element (R3) having an end connected to the anode of the first diode element and the other end connected to the reference voltage output terminal; a first P-type transistor (Tr1) for supplying a current to the reference voltage output terminal; a second P-type (Tr2) transistor having a gate terminal connected to its own drain terminal and to a gate terminal of the first P-type transistor; a bandgap reference circuit (30) having a feedback type control circuit (31) for controlling a drain current of the second P-type transistor such that a voltage at the anode of the first diode element is equal to a voltage at a connection point between the first and second resistive elements; and a start-up circuit (40) for, if an output voltage of the reference voltage output terminal of the bandgap reference circuit is at an abnormal stabilization point, shifting the output voltage from the abnormal stabilization point to a normal stabilization point.

AAPA fails to show that the start-up circuit is between the drain terminal of the second P-type transistor of the reference circuit and the ground potential and, a current consumed by the start-up circuit is supplied from the drain terminal of the second P-type transistor, and if the drain current of the second P-type transistor is substantially zero, the start-up circuit increases the drain current of the second P-type transistor.

However, Chou figure 8 shows a start-up circuit that is between the drain terminal of the second P-type transistor (P2) of the reference circuit and the ground potential and a current consumed by the start-up circuit is supplied from the drain terminal of the second P-type transistor, and if the drain current of the second P-type transistor is substantially zero, the start-up circuit increases the drain current of the second P-type transistor.

Chou teaches in column 7, lines 45 -55 that the start-up circuit's current flow causes the second P-type transistor to turn on to conduct.

Therefore it would have been obvious to one having ordinary skill in the art, at the time of the invention, to use Chou's start-up circuit in place of AAPA start-up circuit with the purpose of reducing noise variations.

As to claim 2, Chou figure 8 shows a reference voltage generation circuit wherein the start-up circuit has P-type transistor (P80) whose gate terminal is connected to the reference voltage output terminal.

It would have been obvious for the reference voltage generation circuit to include a start-up circuit has P-type transistor whose gate terminal is connected to the reference voltage output terminal, for the same reasons stated above.

As to claim 3, Chou figure 8 shows a reference voltage generation circuit wherein the start-up circuit includes a P-type transistor (P80) having a gate terminal connected to the reference voltage output terminal; and a current generating element [P8n]

provided between a source terminal of the P-type transistor and a drain terminal of the second P-type transistor of the reference circuit.

It would have been obvious for the reference voltage generation circuit to include a P-type transistor having a gate terminal connected to the reference voltage output terminal; and a current generating element provided between a source terminal of the P-type transistor and a drain terminal of the second P-type transistor of the reference circuit, for the same reasons stated above.

As to claims 5 and 6, Chou figure 8 shows a reference voltage generation circuit wherein the current generating element is a transistor (P8n) whose gate terminal is connected to a drain terminal. When a transistor has its gate terminal and drain terminal coupled it acts as a diode (Taught in Chou column 7, lines 49 - 51).

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a diode connected transistor, for the same reasons stated above.

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as in view of Chou (US 6,201,435) as applied to claim 3, and in further view of Schrader (US 7,304,595). AAPA and Chou teach all the limitations of claim 3 but fail to teach that the current generating element is a resistive element or a transistor whose gate terminal is fixed to a constant voltage.

However, Schrader figure 1 shows that a current generating element can be a transistor (316) whose gate terminal is fixed to a constant voltage (Vb2). When the gate

terminal is fixed to a constant voltage it acts as a resistor (Taught in 1.1.1 of Design and Analysis of Integrator-Based Log-Domain Filter Circuits)

Schrader teaches in column 4, lines 44 - 49 that the drain of transistors 316 has a high impedance and outputs a current source.

Therefore, it would have been obvious to a person of ordinary skill to try to use the current generating transistor in Schrader in an attempt to provide an improved type of current generating element, as a person with ordinary skill has good reason to pursue known options within his or her technical grasp. In turn, because the transistor as claimed has the properties predicted by Schrader, it would have been obvious to use a transistor that generates current.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brandon S Cole/
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125